

170724110 EFM32G Product Revision E

PRCN Issue Date: 7/24/2017 Effective Date: 10/27/2017

PCN Type: Product Revision

Description of Change

Silicon Labs is pleased to announce product revision E of the Gecko 32-bit MCU devices. This document and description applies to the EFM32GXXX device family. The new revision includes pin-compatible replacements for the previous revision devices and results in updates to the Data Sheet, Reference Manual, and Errata.

With revision E, all Orderable Part Numbers have been consolidated into single documents, Data Sheet rev 2.10, and Errata revision 2.20.

The EFM32GXXX Reference Manual is updated to Rev 1.31.

The updated Errata added ADC E118, DAC E109, EBI E101, and PCNT E102 and it resolved EMU E107. See Errata version 2.20 for complete details.

The Data Sheet changes are summarized below (table numbers refer to EFM32G880 v1.90 datasheet):

- -Added a Feature List
- -Updated Ordering Codes and added Figure 2.1 Ordering Code Decoder
- -Added section 3.1.26 Liquid Crystal Display Driver (LCD) for LCD-enabled devices, due to merged Data Sheet
- -Relabeled Section 2.2 as 3.2, and added separate Configuration Tables for each device (indicated by feature set)
- -Split the Memory Map Figure into two separate figures with peripheral listing and core and code space listing
- -Section 3.1 Test Conditions -
- -Removed note about simulation characterization method
- -Removed footnote about max storage temperature from Absolute Maximum section
- -Table 3.5 Power Management Clarified test conditions for existing BOD threshold rising/falling specifications, and added BOD threshold specs on falling supply for EM1 and EM2
- -Table 3.7 Flash Updated page and device erase time specifications and added footnote for more clarity
- -LFRCO Updated graphs (frequency vs temperature and voltage supply)
- -Table 3.11 HFRCO Increased typical current consumptions, IHFRCO
- -Updated Figures 3.21-3.26 (HFRCO)
- -Table 3.14 ADC -
 - -Added new input bias current (IADCBIASIN) and input offset current (IADCOFFSETIN) specifications
 - -Added conditions for the ADC clock frequency, fADCCLK, at two different BIASPROG settings (7 MHz and 13 MHz)
- -Added new spec conditions for Signal-to-Noise Ratio, SNRADC, at various BIASPROG settings and increased some existing
- -Added new spec conditions for Signal-to-Noise and Distortion Ratio, SINADADC, at various BIASPROG settings and increased some existing specs
- -Added new spec conditions for Spurious-Free Dynamic Range, SFDRADC, at various BIASPROG settings and increased some existing specs
 - -Specified that the min/max Offset Voltage, VADCOFFSET, is for the differential spec instead of the single-ended spec
 - -Updated the unit of measure for the Missing Codes specification
 - -Added the following new specs at each voltage reference (VREF) setting:
 - -Gain error drift, (GAINED)
 - -Offset error drift, (OFFSETED)
 - -Vref voltage, (VREF)
 - -Vref drift, VREF_VDRIFT, due to voltage drift -Vref drift, VREF_TDRIFT, due to temperature drift
 - -Vref current consumption, (IVREF)
 - -ADC and DAC Vref matching, (VREF_MATCH)
 - -Updated table footnotes
- -Table 3.15 DAC
 - -Updated the test condition information for active current, IDAC, for more clarification
 - -Added maximum load current, ILOAD_DC
 - -Added the following new specs at each voltage reference setting:
 - -Vref voltage, (VREF)

 - -Vref drift, VREF_VDRIFT, due to voltage drift -Vref drift, VREF_TDRIFT, due to temperature drift
 - -Vref current consumption, (IVREF)
 - -ADC and DAC Vref matching, (VREF_MATCH)
 - -Updated the footnote for more clarification and to include maximum average active current
- -Table 3.12 ACMP Increased active current for one of the spec conditions
- -Table 3.13 VCMP Increased VCMP hysteresis spec
- -Moved Pinout and Package section to 5.0 and included all device packages, and updated marking figures to include temperature grade
- -Corrected the pin number for symbol P3 for the PCB land pattern dimensions Table for the QFN32 package
- -New document formatting throughout

Refer to the Data Sheet for the complete details.

Revision E introduces an updated orderable part number format with enhanced information fields. Specifically, fields specifying temperature grade and product revision are now included. See Product Identification section of this document for further details.

After the effective date of this PCN, Silicon Labs reserves the right to deliver product revision E for customers ordering product revision D.

Reason for Change

Revision to die to correct errata, improve manufacturability and continuity of supply, and updated specifications based on the results of additional silicon characterization.

Impact on Form, Fit, Function, Quality, Reliability

There is no impact to form, fit, quality or reliability.

The following functions are impacted:

- -Updated device revision information in ROM Table (PID0 PID3 registers)
 -New errata: ADC_E118, DAC_E109, EBI_E101, and PCNT_E102
 -Resolved errata: EMU_E107

Product Identification

Existing Part Numbers Re	enlacement Part Numbers	Drop-in Compatibility
<u> </u>	FM32G200F16G-E-QFN32	See Data Sheet
	FM32G200F16G-E-QFN32R	See Data Sheet
	FM32G200F32G-E-QFN32	See Data Sheet
_	FM32G200F32G-E-QFN32R	See Data Sheet
_	FM32G200F64G-E-QFN32	See Data Sheet
	FM32G200F64G-E-QFN32R	See Data Sheet
	FM32G210F128G-E-QFN32	See Data Sheet
_	FM32G210F128G-E-QFN32R	See Data Sheet
	FM32G222F128G-E-QFP48	See Data Sheet
_	FM32G222F128G-E-QFP48R	See Data Sheet
	FM32G222F32G-E-QFP48	See Data Sheet
	FM32G222F32G-E-QFP48R	See Data Sheet
-	FM32G222F64G-E-QFP48	See Data Sheet
_	FM32G222F64G-E-QFP48R	See Data Sheet
_	FM32G230F128G-E-QFN64	See Data Sheet
_	FM32G230F128G-E-QFN64R	See Data Sheet
_	FM32G230F32G-E-QFN64	See Data Sheet
_	FM32G230F32G-E-QFN64R	See Data Sheet
-	FM32G230F64G-E-QFN64	See Data Sheet
-	FM32G230F64G-E-QFN64R	See Data Sheet
-	FM32G232F128G-E-QFP64	See Data Sheet
•	FM32G232F128G-E-QFP64R	See Data Sheet
•	FM32G232F32G-E-QFP64	See Data Sheet
_	FM32G232F32G-E-QFP64R	See Data Sheet
	FM32G232F64G-E-QFP64	See Data Sheet
_	FM32G232F64G-E-QFP64R	See Data Sheet
_	FM32G280F128G-E-QFP100	See Data Sheet
-	FM32G280F128G-E-QFP100R	See Data Sheet
	FM32G280F32G-E-QFP100	See Data Sheet
_	FM32G280F32G-E-QFP100R	See Data Sheet
	FM32G280F64G-E-QFP100	See Data Sheet
	FM32G280F64G-E-QFP100R	See Data Sheet
EFM32G290F128-BGA112T EI	_	See Data Sheet
	FM32G290F128G-E-BGA112R	See Data Sheet
	FM32G290F32G-E-BGA112	See Data Sheet
	FM32G290F32G-E-BGA112R	See Data Sheet
	FM32G290F64G-E-BGA112	See Data Sheet
	FM32G290F64G-E-BGA112R	See Data Sheet
	FM32G30F128G-E-QFN64	See Data Sheet
_	FM32G30F128G-E-QFN64R	See Data Sheet
-	FM32G800F128G-E-D1I	See Data Sheet
		See Data Sheet
	FM32G840F128G-E-QFN64R	See Data Sheet
	FM32G840F32G-E-QFN64	See Data Sheet
_	FM32G840F32G-E-OFN64R	See Data Sheet
_	FM32G840F64G-E-QFN64	See Data Sheet
_	FM32G840F64G-E-QFN64R	See Data Sheet
_	FM32G842F128G-E-QFP64	See Data Sheet
_	FM32G842F128G-E-QFP64R	See Data Sheet
•	FM32G842F32G-E-QFP64	See Data Sheet
	-	

EFM32G842F32-QFP64	EFM32G842F32G-E-QFP64R	See Data Sheet	
EFM32G842F64-QFP64T	EFM32G842F64G-E-QFP64	See Data Sheet	
EFM32G842F64-QFP64	EFM32G842F64G-E-QFP64R	See Data Sheet	
EFM32G880F128-QFP100T	EFM32G880F128G-E-QFP100	See Data Sheet	
EFM32G880F128-QFP100	EFM32G880F128G-E-QFP100R	See Data Sheet	
EFM32G880F32-QFP100T	EFM32G880F32G-E-QFP100	See Data Sheet	
EFM32G880F32-QFP100	EFM32G880F32G-E-QFP100R	See Data Sheet	
EFM32G880F64-QFP100T	EFM32G880F64G-E-QFP100	See Data Sheet	
EFM32G880F64-QFP100	EFM32G880F64G-E-QFP100R	See Data Sheet	
EFM32G890F128-BGA112T	EFM32G890F128G-E-BGA112	See Data Sheet	
EFM32G890F128-BGA112	EFM32G890F128G-E-BGA112R	See Data Sheet	
EFM32G890F32-BGA112T	EFM32G890F32G-E-BGA112	See Data Sheet	
EFM32G890F32-BGA112	EFM32G890F32G-E-BGA112R	See Data Sheet	
EFM32G890F64-BGA112T	EFM32G890F64G-E-BGA112	See Data Sheet	
EFM32G890F64-BGA112	EFM32G890F64G-E-BGA112R	See Data Sheet	

Last Date of Unchanged Product: 10/27/2017

Qualification Samples

Samples are available upon request

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.

Customer Early Acceptance Sign Off

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance:

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Name:	 	
Company:	 	

Email your early Acceptance approval to: PCNEarlyAcceptance@silabs.com

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Qualification Data

See attached Qualification Report in Appendix

EFM32G Rev E Qualification Report

W7101F1 - Product Qualification Report Record Rev. I

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Part Rev E, T	Part Rev E, TSMC Fabrication						
	T . O . U.I			Fail/Pass or	None	6	Carteria
Test Name	Test Condition	Qualification	Start	End	Notes	Summary	Status
HAST	Accelerated Environment Stress	s Tests - 100-LQ	_				
HASI	JA110		Q034611		1		_
	130°C, 85%RH	3 lots, N=>25	Q034908		1	3 lots	Pass
HACT	Vcc=3.6V, 96 hours		Q034557	0/24	1	0/82	
uHAST	JA118		Q038617	0/30	1		
	130°C, 85%RH	3 lots, N=>25	Q038618	0/30	1	3 lots	Pass
	96 hours		Q040574	0/30	1	0/90	
Temp Cycle	JA104		Q038619	0/30	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q038620	0/30	1	3 lots	Pass
	500 cycles		Q040573	0/30	1	0/90	
HTSL	JA103		Q034614	0/30	1		
	150°C, 1000hr	3 lots, N=>25	Q034995	0/30	1	3 lots	Pass
			Q034560		1	0/90	
	Accelerated Environment Stress	s Tests - 112-LFI	BGA-10x10	- ASEKR			
HAST	JA110		Q040327	0/30	1		
	130°C, 85%RH	3 lots, N=>25	Q040328	0/30	1	3 lots	Pass
	Vcc=3.6V, 96 hours		Q040575	0/30	1	0/90	
uHAST	JA118		Q040331	0/30	1		
	130°C, 85%RH	3 lots, N=>25	Q040332	0/30	1	3 lots	Pass
	96 hours		Q040572	0/30	1	0/90	
Temp Cycle	JA104		Q040329	0/30	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q040330		1	3 lots	Pass
	500 cycles		Q040570		1	0/90	
HTSL	JA103		Q040333		1		
	150°C, 1000hr	3 lots, N=>25	Q040334		1	3 lots	Pass
	130 0, 1000111	5 1013, 11-25	Q040571	0/30	1	0/90	1 033
Test Group A - A	Accelerated Environment Stress	s Tests - 64-TQF			ASEKR	5.00	
HAST	JA110		Q038044		1		
	130°C, 85%RH	3 lots, N=>25	Q038047		1	3 lots	Pass
	Vcc=3.6V, 96 hours		Q038045	0/30	1	0/90	
uHAST	JA118		Q038046	0/30	1	0.00	
	130°C, 85%RH	3 lots, N=>25	Q038049		1		
	96 hours	.510,11 - 20	Q038048		1		
	30 110013		Q040600		1	5 lots	Pass
			Q041162	0/26	1	0/146	1 433
Temp Cycle	JA104	 	Q038052		1	0/140	
-,	Cond C: -65°C to 150°C	3 lots, N=>25	Q038052		1	4 lots	Pass
		3 IOIS, IN-725	Q038050	0/30		4 1005	rass
	500 cycles				1	0/116	
			Q041161	0/26	1	0/116	

Approved by: Vincent Hidajat

1 of 3

Prepared on: 19-May-17

EFM32G Rev E Qualification Report

W7101F1 - Product Qualification Report Record Rev.

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Part Rev E, TS	MC Fabrication						
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
HTSL	JA103	Quantication	Q038054	0/30	1		
	150°C, 1000hr	3 lots, N=>25	Q038055		1	3 lots	Pass
	150 0, 100011	3 lots, IV->25	Q038053	0/30	1	0/90	rass
Test Group A – Acc	celerated Environment Stress	s Tests - 64-VQF				0,00	
HAST	JA110		Q040441		1		
	130°C, 85%RH	3 lots, N=>25	Q040442		1	3 lots	Pass
	Vcc=3.6V, 96 hours	'	Q040443	0/30	1	0/90	
uHAST	JA118		Q040447	0/30	1		
	130°C, 85%RH	3 lots, N=>25	Q040448	0/30	1	3 lots	Pass
	96 hours		Q040449	0/30	1	0/90	
Temp Cycle	JA104		Q040444	0/30	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q040445	0/30	1	4 lots	Pass
	500 cycles		Q040446	0/30	1	0/120	
	'		Q041268	0/30	1		
HTSL	JA103		Q038213	0/30	1		
	150°C, 1000hr	3 lots, N=>25	Q038214	0/30	1	3 lots	Pass
			Q038215	0/30	1	0/90	
Test Group B – Acc	celerated Lifetime Simulation	Tests					
HTOL	JA108		Q040476	0/80			
	T _J ≥ 125°C, Dynamic	3 lots, N=>77	Q040536	0/80		3 lots	Pass
	Vcc=3.6V, 1000 hours		Q040537	0/80		0/240	
LTOL	JA108						
	T _A = -10°C, Dynamic	1 lot, N=>32	Q034510	0/40		1 lots	Pass
	Vcc=3.6V, 1000 hours					0/40	
ELFR	JA108		Q040408	0/503			
	T _J ≥ 125°C, Dynamic	3 lots, N=>500	Q040315	0/503		3 lots	Pass
	Vcc=3.6V, 48 hours		Q040535	0/503		0/1509	
Data Retention	AEC-Q100-005		Q037807	0/40			
High Temp	150°C, 1000 hours	3 lots, N=> 39	Q038151	0/40		3 lots	Pass
			Q038112	0/40		0/120	
Data Retention	AEC-Q100-005		Q037754	0/40			
Low Temp	25°C, 1000 hours	3 lots, N=> 38	Q038152	0/40		3 lots	Pass
			Q038150	0/40		0/120	
NVM P/E Cycling	AEC-Q100-005		Q037702	0/40			
High Temp	85°C, 24 hours	3 lots, N=> 77	Q038086	0/40		3 lots	Pass
			Q038119	0/40		0/120	
NVM P/E Cycling	AEC-Q100-005		Q038120	0/40			
Low Temp	25°C, 24 hours	3 lots, N=> 77	Q038113	0/40		3 lots	Pass
			Q037703	0/40		0/120	

Approved by: Vincent Hidajat

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Rev. I

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Part Rev E, TSMC Fabrication								
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status	
Test Group E – I	Test Group E – Electrical Verification							
ESD-HBM	JS-001	1 lot, N=>3	Q040266			2000 V	Class 1C	
ESD-CDM	JS-002	1 lot, N=>3	Q040267 Q040632 Q040477 Q041189 Q038043 Q041091		3 4 5 6 7 8	500 V 500 V 750 V 750 V 750 V 750 V	Class C2A Class C2B Class C2B Class C2B Class C2B Class C2B	
Latch Up	JESD78 ±200mA Overvoltage = 3.8V	1 lot, N=>3	Q040265 Q040264		2 2		Pass	

Notes:

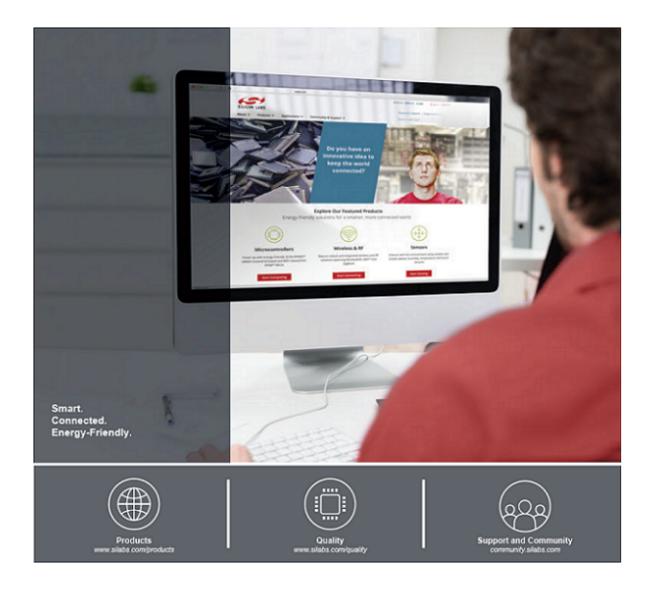
- 1. Parts are Pre-conditioned at MSL3/260°C
- 2. All pins passed ±200mA except pin PA12 / PA13
- 3. 112-LFBGA-10x10 ASEKR
- 4. 100-LQFP-14x14 ASECL
- 5. 64-VQFN-9x9 ASEKR
- 6. 32-VQFN-6x6 ASEKR
- 7. 64-TQFP-10x10 ASEKR
- 8. 48-TQFP-7x7 ASEKR

T	his report applies to the following part numbe	ers:
EFM32G280F32G-E-QFP100	EFM32G230F32G-E-QFN64	EFM32G290F32G-E-BGA112
EFM32G280F64G-E-QFP100	EFM32G230F64G-E-QFN64	EFM32G290F64G-E-BGA112
EFM32G280F128G-E-QFP100	EFM32G230F128G-E-QFN64	EFM32G290F128G-E-BGA112
EFM32G880F32G-E-QFP100	EFM32G840F32G-E-QFN64	EFM32G890F32G-E-BGA112
EFM32G880F64G-E-QFP100	EFM32G840F64G-E-QFN64	EFM32G890F64G-E-BGA112
EFM32G880F128G-E-QFP100	EFM32G840F128G-E-QFN64	EFM32G890F128G-E-BGA112
EFM32G230F32G-E-QFN64	EFM32G200F16G-E-QFN32	EFM32G222F32G-E-QFP48
FM32G230F64G-E-QFN64	EFM32G200F32G-E-QFN32	EFM32G222F64G-E-QFP48
EFM32G230F128G-E-QFN64	EFM32G200F64G-E-QFN32	EFM32G222F128G-E-QFP48
EFM32G232F32G-E-QFP64	EFM32G210F128G-E-QFN32	
EFM32G232F64G-E-QFP64		
EFM32G232F128G-E-QFP64		

Approved by: Vincent Hidajat

3 of 3

Prepared on: 19-May-17



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